Amendments to the Specification:

Please rewrite paragraph 17 on page 5 as follows:

The output circuit 130 generally comprises a data input pointer circuit 132 and a data output pointer circuit 134. The data input pointer circuit receives a data input enable signal FI from the read timer 102 and generates an input pointer 135, while the data output pointer circuit receives a data output enable signal FO from the CAS latency logic circuit 137 and generates an output pointer 138. The output signals of the CAS latency logic circuit (FO) are derived from a delay-lock loop 136, the programmed CAS latency and the internal generated READ signal. The input pointer 135 and the output pointer 138 are coupled to the decoder 140. The decoder 140 uses the pointers to generate an input address 142 and an output address 144 respectively to properly address a FIFO buffer 144. That is, the decoder generates the appropriate address in the FIFO buffer based upon the input pointer 135 for data that is read from the memory elements 121, and generates the appropriate address to output data from the memory device based upon the output pointer 138. Finally, the output data 148 is coupled to an off chip driver (OCD) 150 and a contact pad 152.

Please rewrite paragraph 21 on page 7 as follows:

The delayed-lock loop circuit 302 further generates a plurality of delayed clock signals which are coupled to a synchronization circuit 320. The synchronization circuit comprises logic circuits 322-326. Each logic circuit receives a synchronization enable signal and a delayed clock signal, and generates an enable signal. The synchronization enable signal is derived by the CAS latency logic circuit 360 which receives a delayed clock signal from delay line element 312, the CAS latency information and the internal generated READ signal. The CAS latency logic circuit also generates a data output enable signal FO. In particular, a first logic circuit 322 receives the synchronization enable signal and a delayed clock signal from delay line element 306 to generate a read enable signal READ1. Similarly, a second logic circuit 324 receives the synchronization enable signal and a delayed clock signal from delay line element 308 to generate a read enable signal READ2. The read enable signals READ1 and READ2 are coupled to a

read circuit 330 which reads data from memory elements 331. The read circuit 330 comprises a secondary sense amplifier 332 coupled to a driver 334. The driver 334, which is enabled by the READ1 signal, provides an output to a multiplexer 336. The multiplexer 336 provides an output to a second driver 338 enabled by the READ2 signal. Finally, a third logic circuit 326 receives synchronization enable signal and a delayed clock signal from delay line element 310 to generate a data input enable signal FI.

Please rewrite the Abstract as follows:

~~The present invention relates to a memory device which enables a greater amount of time to read data into a buffer. In particular, a~~A memory device ~~according to one aspect of the present invention comprises~~ includes a delay-locked loop circuit having ~~a plurality of~~ delay elements and a synchronization circuit coupled to the delay-locked loop circuit. The synchronization circuit ~~also~~ receives a synchronization enable signal and outputs a plurality of enable signals, including an enable signal coupled to an output circuit. Because the enable signal ~~coupled to the output circuit~~ is synchronized with the read signal, it is possible to provide more time to read data into the buffer. ~~According to another aspect of the present invention, a~~A method of reading data from a memory device couples a synchronization enable signal and an external clock signal to a synchronization circuit. ~~An external clock signal is also coupled to a delay-locked loop circuit.~~ A read signal ~~is~~ and an output enable are generated based upon a synchronization enable signal and a delayed clock signal of the external clock signal. ~~An output enable is also generated based upon the synchronization enable signal and a delayed clock signal of the external clock signal.~~ Because the output signal is synchronized to the read signal, more time is allowed for the sense function.